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Direct interface for capacitive sensors based on the charge transfer method

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Abstract – We present the theoretical analysis and experimental performance results of a direct interface for capacitive sensors based on the charge transfer method when parasitic capacitances are included. The interface circuit implements a two-point calibration technique that makes measurement results independent from voltage- and temperature-dependent parameters. The measurement deviation is below 1 % FSR (Full Scale Range) for capacitances from 10 pF to 1 nF.

Keywords – Direct sensor interface, capacitive sensor, charge transfer method, microcontroller, capacitance measurement.

I. INTRODUCTION

In recent years, some interface circuits for capacitive sensors have been implemented where the sensor is directly connected to a microcontroller (MCU). The MCU performs the capacitance-to-digital conversion without any external circuit for signal conditioning or analog-to-digital voltage conversion. Hence, these interface circuits are compact and inexpensive.

Direct capacitance-to-digital conversion relies on voltage comparison and timing. Reverter et al. [1] implemented a direct interface circuit based on measuring the discharging time of an *RC* circuit that included the capacitive sensor. For a measurement range from 10 pF to 100 pF, the measurement deviation was below 1.5 % FSR. Nevertheless, to obtain the best speed-resolution trade-off when measuring in the picofarad range, they required a resistor larger than 10 MΩ, which increased the sensitivity to noise and external interference. Hence, capacitive sensors with large electrodes cannot be easily measured with this method.

Dietz et al. [2] proposed an alternative circuit based on the charge transfer method, where the unknown capacitance is calculated by counting the number of charge transfer cycles needed to charge a reference capacitor to a threshold voltage via the capacitive sensor. In contrast with [1], the interface circuit did not include any resistor, so its susceptibility to noise and external interference should be lower. However, no quantitative information about circuit performance was provided.

Blake et al. [3] implemented a direct interface circuit that combined both techniques: the unknown capacitance was measured by the charge transfer method, and the circuit was calibrated by an *RC* network with a known *R*. For capacitances below 300 pF, the measurement deviation was less than 10 % FSR.

Whatever the method, direct interface circuits for capacitive sensors are sensitivity to parasitic capacitances, which increases the measurement uncertainty especially when measuring in the picofarad range. These parasitic capacitances mainly depend on the layout on the printed circuit board and on the wiring between sensor and the microcontroller, and their effects can be reduced by calibration [1].

This paper presents the theoretical analysis and experimental performance results of the direct interface circuit proposed in [2], when measuring in the range from 10 pF to 1 nF with a two-point calibration technique [4], and the effects of parasitic capacitance are included.

II. INTERFACE CIRCUIT DESCRIPTION

A. Operating principle

Figure 1 shows the operating principle for capacitance measurement based on the charge transfer method. It can be analyzed as a switched capacitor *RC* circuit [5] where C_x is the unknown capacitance, C_r is the reference capacitance, and V_S the source voltage. All of them are assumed to be constant.

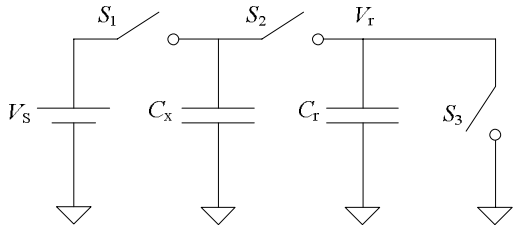

Fig. 1. Capacitance measurement circuit based on the charge transfer method.

The operation sequence is as follows. First, switch S_3 closes to reset C_r. Then, S_3 opens and S_1 closes, and C_x is charged to V_S. Next, S_1 opens and S_2 closes, so that the charge stored on C_x is shared with C_r, which results in a voltage across C_r directly proportional to the charge transferred from C_x to C_r. By repeating the charge transfer cycle, C_x exponentially charges C_r towards V_S. This implies that C_r must be higher than C_x. From here, C_x can be determined by counting the number of charge transfer cycles needed to charge C_r to a given threshold voltage V_T.

The voltage across C_r at any arbitrary N charge transfer cycle is

$$V_r[N] = \frac{C_x}{C_x + C_r} V_S + \frac{C_r}{C_x + C_r} V_r[N-1] \quad (1)$$

If we assume $V_r[0] = 0$ because of the initial closing of S_3, by summing the geometric progression we obtain,

$$V_r[N] = V_S \left[1 - \left(\frac{C_r}{C_x + C_r} \right)^N \right] \quad (2)$$

From here, considering $C_r >> C_x$, we obtain

$$N = -\frac{1}{C_x} C_r \ln\left(1 - \frac{V_T}{V_S}\right) \quad (3)$$

that can be rearranged as

$$C_x = \frac{k}{N} \quad (4)$$

where $k = -C_r \ln(1 - V_T/V_S)$. From (3), N increases at a rate proportional to C_r/C_x.

B. Interface circuit

Figure 2 shows the interface circuit proposed in [2] plus parasitic capacitances to ground C_{p0} and C_{p1}. C_x is the capacitance to be measured; C_r is the reference capacitor; C_{p0} and C_{p1} model the parasitic capacitances from nodes 0 and 1 to ground, respectively; R_{OL} and R_{OH} model the channel resistance of the transistor of the output buffer when it provides a digital "0" and a digital "1", respectively; the values of this resistances can be assumed constant whenever the transistor works in its ohmic region [6]. V_{OL} and V_{OH} are the output voltage levels when it provides a digital "0" and a digital "1" respectively.

From the operating principle explained in the Section II.A, the measurement method involves three stages: reset (only at the beginning of the measurement), charging, and transferring. During the resetting stage (Fig. 2a), pins 0 and 1 are set as an output that provides a digital "0" and C_r is discharged towards V_{OL} through R_{OL}. Hence, $V_r[0] \approx 0$. During the charging stage (Fig. 2b), pin 0 provides a digital "1" and pin 1 is set as an input (high-impedance input Z_i). Therefore, C_x is charged towards V_{OH} through R_{OH}. Also C_r is slightly charged towards V_{OH} due to C_{p1}. During the transferring stage (Fig. 2c), pin 0 is set as an input (to act as a threshold detector), pin 1 is set as an output that provides a digital "0", and the control program starts counting the number of charge transfer cycles. In this condition, C_x shares its charge Q_x with C_r, previously charged at Q_r. The charge transfer cycling is repeated until the voltage across C_r reaches the trigger level V_T of the input buffer. According to the analysis described in the Appendix, from (A6) we obtain

$$N = \frac{\ln\left(1 - \frac{V_T}{V_{OH}}\right)}{\ln\left[\frac{C_r^2}{(C_x + C_{p0} + C_r)(C_r + C_{p1})}\right]} \quad (5)$$

and considering $C_r >> C_x$, C_{p0}, C_{p1}, we obtain

$$C_x = \frac{k}{N} - (C_{p0} + C_{p1}) \quad (6)$$

where $k = -C_r \ln(1 - V_T/V_{OH})$. V_{OH} and V_T depend on the supply voltage; further, they all drift with temperature.

The time duration of each stage of the measurement process must be long enough to ensure that the final voltage across capacitances is close enough to its ideal value. Selecting $T_D \geq 10 R_{OL} C_r$ for the resetting stage, $T_C \geq 10 R_{OH} C_x$ for the charging stage, and $T_R \geq 10 R_{OL} C_x$ for the transferring stage, results in a relative deviation below 4.5×10^{-5}.

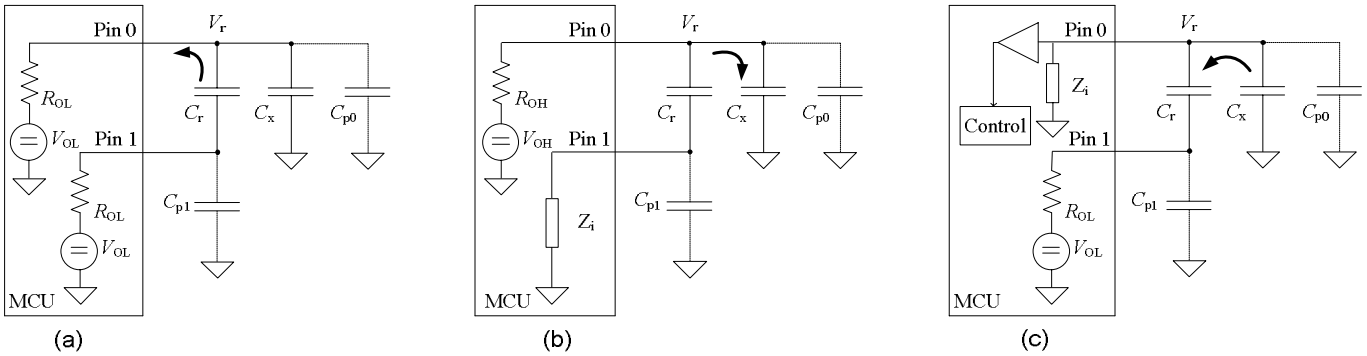

Fig. 2. Direct interface for a capacitive sensor based on the charge transfer method. (a) Resetting stage (only at the beginning of the measurement). (b) Charging stage. (c) Transferring stage.

C. Calibration technique

Calibration makes measurement results independent from V_{OH}, V_T, and C_r, hence from k. Because stray capacitances add a zero effect to the transfer characteristic in (6), we can also expect to reduce that effect by calibration. So, a two-point calibration technique can compensate for these two effects.

Figure 3 shows the proposed interface circuit with two calibration points. Only parasitic capacitances to ground have been included, because use to be the larger stray capacitances. This calibration technique implies three measurements, one for each reference capacitor (C_{c1}, C_{c2}) and one for the unknown capacitance (C_x).

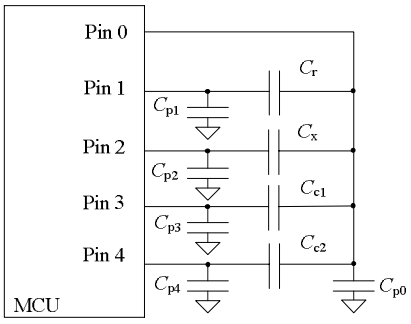

Fig. 3. Interface circuit to implement a two-point calibration technique when parasitic capacitances to ground are included.

Applying to each capacitor the method described in the Section II.B, we obtain

$$C_x = \frac{k}{N_x} - C_{eq\text{-}x} \tag{7a}$$

$$C_{c1} = \frac{k}{N_{c1}} - C_{eq\text{-}c1} \tag{7b}$$

$$C_{c2} = \frac{k}{N_{c2}} - C_{eq\text{-}c2} \tag{7c}$$

where N_x, N_{c1}, and N_{c2} are the number of charge transfer cycles for, respectively: (a) the unknown capacitance C_x, (b) the first reference capacitor C_{c1}, and (c) the second reference capacitor C_{c2}; $C_{eq\text{-}x}$, $C_{eq\text{-}c1}$, and $C_{eq\text{-}c2}$ model the equivalent parasitic capacitances when measuring N_x, N_{c1}, and N_{c2}, respectively. If we assume that k remains the same over the time for the three measurements and $C_{eq\text{-}x} \approx C_{eq\text{-}c1} \approx C_{eq\text{-}c2}$, solving (7) for C_x, yields

$$C_x = \frac{1}{N_x}\frac{N_{c1}N_{c2}}{N_{c1}-N_{c2}}\left(C_{c2}-C_{c1}\right) - \frac{N_{c2}C_{c2}-N_{c1}C_{c1}}{N_{c1}-N_{c2}} \tag{8}$$

which is independent from k and from the parasitic capacitances. By comparing with (6) we see that gain uncertainty has been reduced because the gain now depends on known parameters, and that offset effects have been reduced because they do not include any stray capacitance.

III. MATERIALS AND METHOD

The circuit interface proposed in Fig. 3 has been implemented by using a PIC16F84A MCU, operating at 4 MHz in crystal oscillator mode. The function of pins 0, 1, 2, 3 and 4 were implemented by pins RB0, RB1, RB3, RB4 and RB7 respectively. The control program was written in assembler language. The instruction cycle time was 1 µs, one-fourth of the main oscillation period.

The proposed interface circuit was applied to measure capacitors from 10 pF to 1 nF. All of them were ceramic capacitors with 10 % tolerance. C_r was 1 µF ± 0.1 µF with metallized polyester dielectric. Actual C_x and C_r values were measured by an impedance analyzer (Agilent 4294A) connected to a test fixture (Agilent 16047E). The basic uncertainty of the impedance analyzer is below 1 % in the measurement range from 10 pF to 1 nF, when measuring at 100 kHz and 0.5 V (rms oscillator output level) [8]. T_D, T_C and T_R were calculated via R_{OL} and R_{OH} for pins RB0, RB1, RB3, RB4, and RB7, which were indirectly measured by the voltage-divider technique describe in [6].

The interface circuit was evaluated for two measurement sub-ranges: from 10 pF to 100 pF, and from 100 pF to 1 nF. For C_{c1} and C_{c2} we selected the end values of each sub-range. For each capacitor C_x, C_{c1}, and C_{c2}, the MCU consecutively measured N_x, N_{c1}, and N_{c2} 100 times. The values obtained were sent to a personal computer via a serial link (EIA-232) implemented with a MAX233 under LabVIEW control. Then, 100 values of C_x were calculated by applying (8) and its mean value was calculated. The measurement accuracy was evaluated as the deviation of the mean value from the actual value.

To design the circuit interface the following guidelines were followed:

1. To avoid large parasitic capacitances, C_x, C_{c1} and C_{c2} were placed as close as feasible to the MCU.
2. To reduce the effects of external interference, the unused I/O pins of the MCU were configured as inputs and connected to ground. Further, the printed circuit board did not have any ground plane.
3. To reduce the effects of power supply noise, the MCU and MAX233 were supplied by two independent voltage regulators (LM7805). Moreover, a decoupling capacitor C_d = 100 nF was connected between the MCU power supply pin and ground [6].

IV. EXPERIMENTAL RESULTS AND DISCUSSION

The interface circuit in Fig. 3 was first characterized by measuring some of its parameters according to the procedure

described in Section III. The experimental results were as follows. The internal output resistance for pins RB0, RB1, RB3, RB4 and RB7, when they provide a digital "0" or a digital "1", were below 50 Ω and 125 Ω, respectively. $C_{x,\text{-max}}$ and C_r were 0.96 nF and 1.06 µF, respectively. Consequently, T_D, T_C and T_R should be larger than 0.53 ms, 1.2 µs and 0.48 µs, respectively. However, we selected T_D = 1 s to reduce any possible dielectric absorption effects in C_r [7]. T_C and T_R were selected 5 µs and 25 µs, respectively, by considering the minimal number of instructions to execute at each stage. Figure 4 shows the measurement deviation achieved for each of the ten measured capacitors, which is below 1 %FSR for 10 pF < C_x < 1 nF. These deviations are acceptable for many industrial applications and are smaller than those reported in the bibliography for other direct interface circuits. Moreover, they were obtained without shielding the circuit, which means that the measured sensors can have large dimension, e.g. strip electrodes.

V. CONCLUSIONS

The charge method offers a simple, compact, and low-cost solution to directly connect capacitive sensors to microcontrollers. A theoretical analysis shows the relevant MCU parameters involved, and the effects of parasitic capacitances on the transfer characteristic. A calibration circuit with two known capacitors reduces these effects. The interface circuit has been evaluated by using a low cost MCU (PIC16F84A) and applying some design guidelines. For capacitors from 10 pF to 1 nF, the measurement deviation was below 1 %FSR. This value is acceptable for many applications and it was obtained without any circuit shielding.

APPENDIX

Referring to Fig. 2b, at any arbitrary charge transfer cycle, the charge stored on the parallel combination of C_x and C_{p0} is

$$Q_x[N-1/2] = V_{OH}(C_x + C_{p0}) \tag{A1}$$

In this same stage, the combination of C_r and C_{p01} is also charged. This charge is

$$Q_r[N-1/2] = V_r[N-1/2]C_r \tag{A2}$$

where V_r [N–1/2] is

$$V_r[N-1/2] = \frac{C_r}{C_r + C_{p1}} V_r[N-1] + \frac{C_{p1}}{C_r + C_{p1}} V_{OH} \tag{A3}$$

During the transferring stage, Q_x [N–1/2] and Q_r [N–1/2] are shared. So, the voltage across C_r at the end of charge transfer cycle is

$$V_r[N] = \frac{Q_x[N-1/2] + Q_r[N-1/2]}{C_x + C_{p0} + C_r} \tag{A4}$$

Substituting (A1) and (A2) in (A4), we obtain

$$V_r[N] = \frac{V_{OH}}{C_x + C_{p0} + C_r}\left(C_x + C_{p0} + \frac{C_r C_{p1}}{C_r + C_{p1}}\right) + \frac{{C_r}^2}{(C_x + C_{p0} + C_r)(C_r + C_{p1})} V_r[N-1] \tag{A5}$$

Then, applying sum of geometric progression and assuming $V_r[0] = 0$ we obtain

$$V_r[N] = V_{OH}\left\{1 - \left[\left(\frac{C_r}{C_x + C_{p0} + C_r}\right)\left(\frac{C_r}{C_r + C_{p1}}\right)\right]^N\right\} \tag{A6}$$

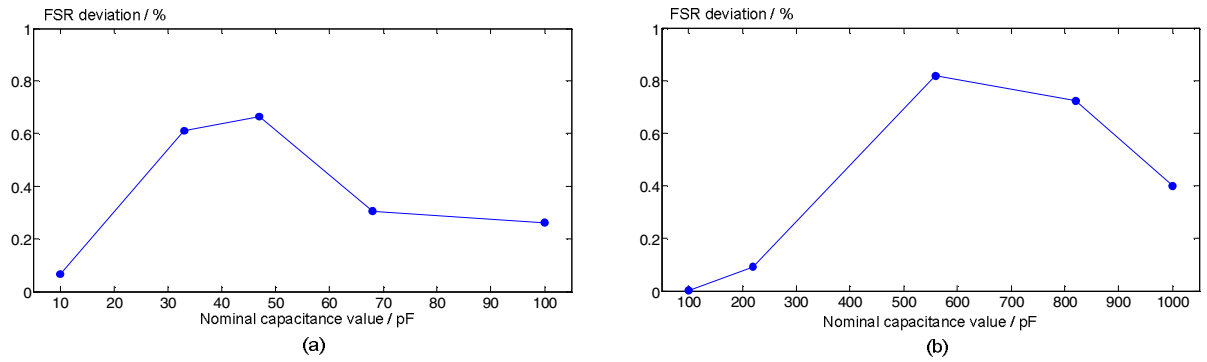

Fig. 4. FSR deviation for measured capacitance from: (a) 10 pF to 100 pF, and (b) 100 pF to 1 nF.

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